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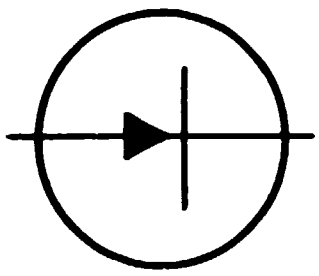

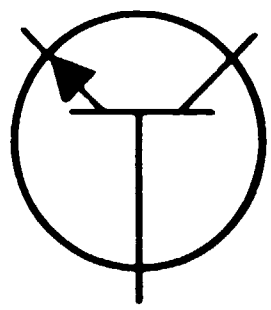

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DESIGN AND DEVELOPMENT OF A HIGH POWER, LOW SATURATION VOLTAGE SILICON SWITCHING TRANSISTOR

Quarterly Report No. 3

Issued July 1968

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

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I. INTRODUCTION

Theoretical considerations indicated the feasibility of developing a transistor with a saturation voltage of 0.1 volt at 75 amperes collector current. This was to be accomplished by making emitter and collector junctions as nearly symmetrical as possible in order to equalize the junction voltages. Practical experience on the contract has indicated that technical difficulties with the original approaches resulted in low gain and/or voltage. Since some of these technical difficulties can be circumvented by the use of the epitaxial base process, it was decided that this approach should be used for the remainder of the project.

II. PROGRESS DURING THE CURRENT QUARTER

A. ANALYSIS OF TECHNICAL APPROACHES

In order to reduce the saturation voltage of a transistor, one looks for improvements in each of the following areas:

(1) reduction of bulk resistances
(2) equalization of junction voltages
(3) increase dc current gain

The approaches originally selected for this contract were aimed at improvement of one or more of the above characteristics. Experience in the early part of the contract indicated that high gain appears to be the most important of these characteristics. This is clearly demonstrated in Figure 1 which is a scatter plot of h_{FE} vs $V_{CE(sat)}$ for 19 transistors. The best fit line* indicates that a gain of 40 at 75A I_C is a minimum requirement for approaching 0.1V $V_{CE(sat)}$.

The strengths and weakness of the three original approaches will be discussed as well as the reasons for selecting the epitaxial base process for the remainder of the contract.

1. Thin Wafer Approach

The use of thin (2-2.5mil) silicon wafers as outlined in Quarterly Report No. 1 seems to be a logical approach to fabricating a low saturation resistance transistor. The use of this material should permit steeper concentration gradients, thereby increasing injection efficiencies as well as reducing series resistance in emitter and collector regions. The validity of this reasoning was demonstrated on small chips (see Tables 1 and 2).

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* Best fit line estimated according to a method of Quenoille, M. H., Rapid Statistical Calculation, Hafner, N. Y., 1959, Method 33.

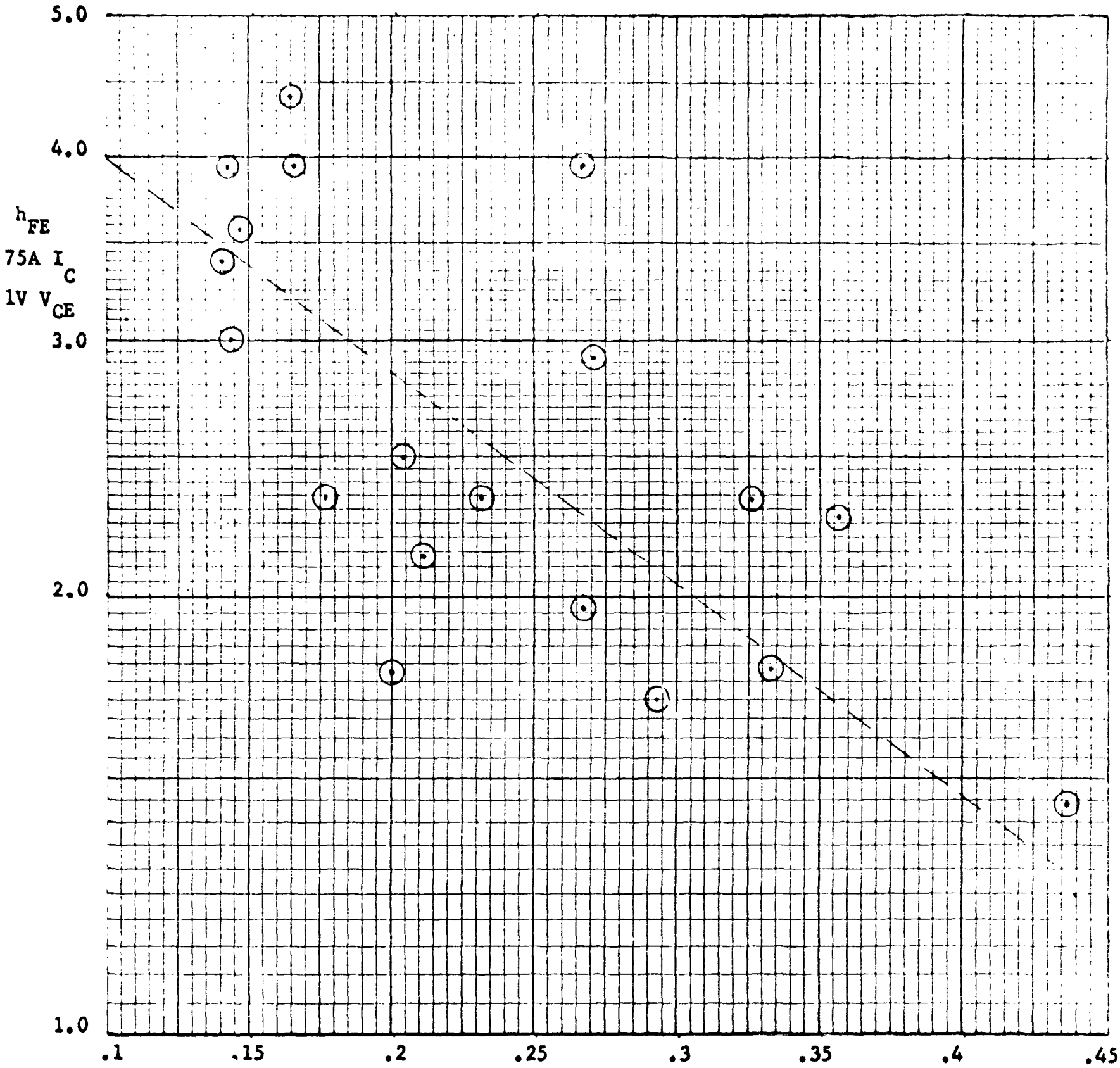

Figure 1. Scatter Plot of h_{FE} vs. $V_{CE(sat)}$

Table 1

Electrical Data - Thin Wafer Transistors

Unit No.	V_{CBO}	I_{CBO}	V_{CEO}	I_{CEO}	V_{EBO}	I_{EBO}	h_{FE} 5A I_C 1V V_{CE}	5A I_C $V_{CE(sat)}$	3A I_B $V_{BE(sat)}$	5A I_C $V_{CE(sat)}$	.5A I_B $V_{BE(sat)}$
1	33V	1 ma	14V	1 ma	11.5V	.01 ma	192	.22	1.05	.23	1.1
2	75V	1 ma	11V	1 ma	11.5V	.01 ma	119	.23	1.05	.23	1.1
3	44V	1 ma	23V	1 ma	10.0V	.01 ma	94	.26	.98	.26	1.0
4	80V	1 ma	14V	1 ma	11.0V	.01 ma	125	.25	1.1	.25	1.1
5	40V	1 ma	15V	1 ma	12.0V	.01 ma	179	.28	1.1	.29	1.2
6	70V	1 ma	28V	1 ma	9.0V	.01 ma	104	.23	.97	.23	1.0
7	94V	1 ma	25V	1 ma	11.5V	.01 ma	88	.22	.94	.21	.96
8	80V	1 ma	12V	1 ma	10.5V	.01 ma	81	.30	1.05	.30	1.1
9	38V	1 ma	27V	1 ma	10.0V	.01 ma	131	.26	1.0	.24	1.05
Mean	61.5V		18.8V		10.8V		123.7	.250	1.027	.248	1.068
Std. Dev.	22.7V		6.8		.97V		39.0	.028	.057	.030	.073

Table 2

Electrical Data - Experimental Control Run

Unit No.	V_{CBO}	I_{CBO}	V_{CEO}	I_{CEO}	V_{EBO}	I_{EBO}	h_{FE} 5A I_C 1V V_{CE}	5A I_C $V_{CE(sat)}$	.3A I_C $V_{BE(sat)}$	5A I_C $V_{CE(sat)}$	.5A I_B $V_{BE(sat)}$
1	38V	1 ma	25V	1 ma	13V	.01 ma	31	.32	.95	.30	.99
2	26V	1 ma	12.5V	1 ma	13V	.01 ma	49	.28	.96	.27	.99
3	19V	1 ma	5.5V	1 ma	13V	.01 ma	43	.32	.99	.32	1.0
4	28V	1 ma	13.5V	1 ma	14V	.01 ma	50	.24	.92	.24	.95
5	20V	1 ma	6.0V	1 ma	10V	.01 ma	54	.21	.90	.21	.92
6	27V	1 ma	13.0V	1 ma	14V	.01 ma	59	.30	.98	.30	1.0
7	36V	1 ma	23.0V	1 ma	13V	.01 ma	41	.37	.95	.32	.98
8	25V	1 ma	11.0V	1 ma	14V	.01 ma	59	.24	.95	.24	.98
9	28V	1 ma	15.0V	1 ma	6V	.01 ma	34	.34	.98	.32	1.0
Mean	27.4V		13.8V		12.2V		46.7	.291	.953	.280	.979
Std. Dev.	6.3V		6.6V		2.6V		10.2	.053	.029	.042	.027

Fabrication of thin wafer devices large enough to meet the requirements of this contract present special problems listed below:

a. Breakage is a very severe problem making it very difficult to get a whole slice through the entire process.

b. Flatness of these wafers may be a problem, especially in those cut to final size by the silicon supplier.

c. The presently used method of mounting the silicon to the molybdenum disc is not suitable since alloying occurs through the entire thickness of the wafer. Development of an alternate mounting technique is beyond the scope of this contract.

These problems are considered great enough to discontinue effort on this approach.

2. Symmetrically Diffused Approach

In order to achieve high gain at high current with the single diffused process, it is necessary to work with base widths of 10μ or less. Historically this has been difficult to achieve, and in this contract the problem was traced to a lack of slice flatness.

The crystal surface of the starting material has been rechecked recently with a newly available Talysurf Model 4 surface contour tester made by Engis Equipment, Inc. A data record is shown in Figure 2. Note that the vertical scale is approximately 400 times the horizontal scale. One si of the surface appears to have a curvature as shown. Within the active transistor region a thickness variation of 0.4 mil out of approximately 6 mils is noted. It can be seen that if a transistor were made on this slice and a base width of 10μ (0.4 mil) were achieved near the central base contact area, the device would be shorted in at least one spot near the edge. Figure 3 shows a cross section of a device in which curvature of the surface did cause the shorting near the edges. This difficulty occurs whether the collector is selective or nonselective.

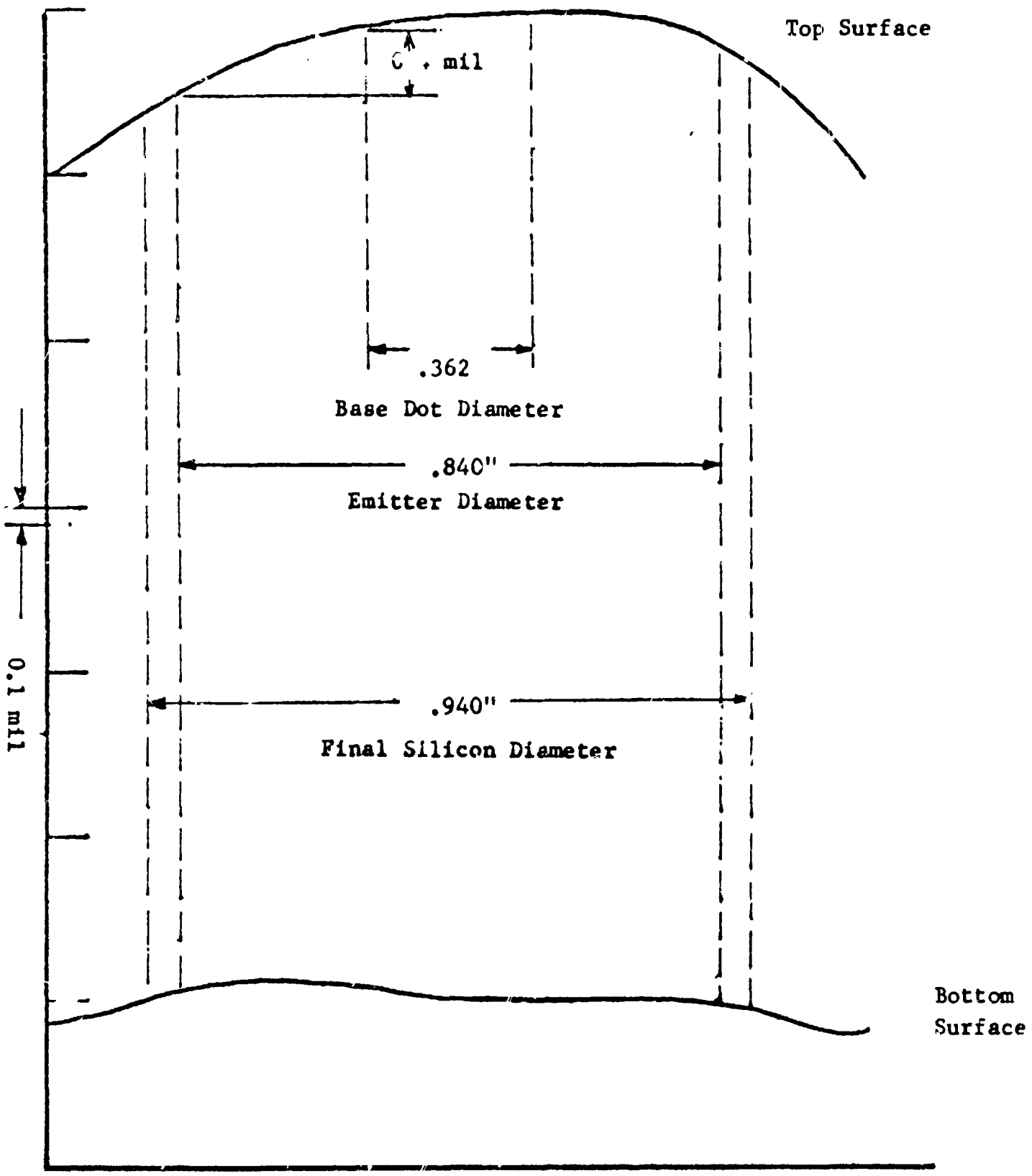

Figure 2

Schematic Representation of Wafer Cross Section

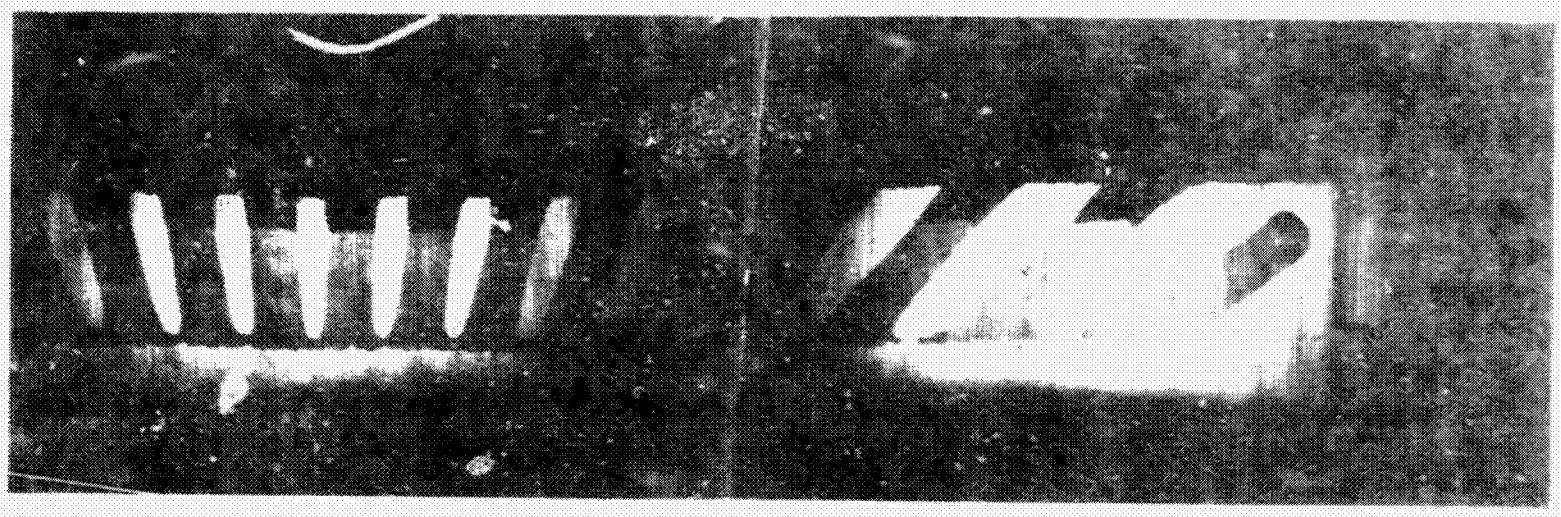

Figure 3

Cross Section of Device Showing
Effect of Surface Curvature

Even in the case where material of improved flatness is available, the degree of control needed in slice thickness measurement and in the deep diffusions does not make this a suitable process for manufacturing.

3. Epitaxial Selective Collector Approach

A proposed method of forming a selective collector epitaxially was outlined in Quarterly Report No. 1. All attempts at forming a selective collector using arsenic diffusion before epitaxy were thwarted by autodoping from the arsenic diffused areas. Since any epitaxial development beyond simple changes in thickness and resistivity of the deposited layers is outside the scope of this contract, this approach has also been abandoned.

4. Epitaxial Base Approach

The course of action selected as an alternative to the three original approaches is the epitaxial base approach. The process itself is not new as it is used on the 176 family and was tried on original Contract No. JPL-951303. The application of the epi base technique to this contract embodies several important differences.

In the original contract, a thin P-layer was grown directly on the N-type, 0.01 ohm-cm substrate. These units had very low breakdown voltages. The design for this contract utilizes epitaxial collector layers of 1 ohm-cm, N-type silicon approximately 10μ thick. This design is expected to relieve the voltage breakdown problem without reducing the high current gain as much as the standard collector layer used on the 170 family would.

The second significant difference is that the base regions will be thicker and of higher resistivity than used on the 170 family. This difference should be helpful in obtaining the "100% yield" needed to produce a single device per slice.

The reasons for selecting the epi base approach are as follows:

a. All operations are performed from the same side of the wafer; that is, epitaxial growth and emitter diffusion are done only on one surface. Both of these processes tend to follow the contour of the surface, thus the final base width should be relatively uniform and independent of slice thickness.

b. Epitaxial base transistors tend to have less fall-off of gain with increasing collector current, thus it should be easier to produce high gain transistors.

c. The "manufacturability" of epi base transistors has been demonstrated on the 170 line, thus a transistor developed on this program would be more than a laboratory curiosity.

B. PROCESSING

Three epitaxial structures were selected for the initial investigation. All of these have an N-type, 0.01 ohm-cm substrate and a 10μ thick collector layer of 1 ohm-cm, N-type silicon. Three different types of base layers were specified as follows:

Type A: 6μ of 1 ohm-cm, P-type
Type B: 15μ of 5 ohm-cm, P-type
Type C: 35μ of 20 ohm-cm, P-type

The purpose of these structures was to permit evaluation of three types of transistor structures; namely, a narrow base, fast switching transistor similar to the Ⓜ 170 family, a wide base transistor similar in performance to the thin wafer, single diffused transistor, and a medium speed compromise between the two extremes.

Difficulty has been experienced in growing the thick layers required for the "C" approach casting doubt on the suitability of that approach for this program.

Attempts are being made to evaluate the slice-to-slice variation of the base layer thickness. These measurements are performed by standard bevel and stain techniques on the annular sections left over after the usable 0.940" diameter section is cut from the center of the 1.3" diameter slice. Thus the measurement can be made without sacrificing usable epi slices. Some preliminary results are presented below (data represents base layer thickness in microns):

Group	Mean	Std. Dev.	Maximum	Minimum	Range
1	4.600	0.310	5.100	4.200	0.900
2	6.050	0.641	6.600	5.100	1.500
3	11.050	1.046	12.000	9.600	2.400
4	17.850	1.618	19.800	15.600	4.200

The target value for Groups 1 and 2 was 5μ, while the target for Groups 3 and 4 was 15μ. The precision with which the target value is achieved is expected to improve when the final design is selected and the process becomes routine. The variation of base depth within a run is less than ±10% for one standard deviation, affording for better control than is possible with the single diffused process.

C. CONTACT RESISTANCE

Although investigation of contact resistance was not a part of the development effort, an improvement was made during this period. A special "window" package was made which allowed measurement of voltage drop within the encapsulation. It was found on one device that a voltage drop of 16.4 mV existed between the moly disc and the mounting foil. When gold plated moly discs were employed, this voltage drop fell below 0.1 mV. In addition, the gold plating improved wetting of the solder to the disc.

III. PROGRAM FOR NEXT PERIOD

Processing will be continued on epitaxial base transistors. Final design will be determined, and transistors will be fabricated to meet the final sample commitment.